Lab3:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Minimum | Typical | Maximum | Units | Description |
| FPGA\_C |  | 0(low) |  | V/logic | On Board Clock |
| S0 |  | 0(low) |  | V/logic | On Board Button, for reset |
| Seg\_1 |  | 0(low) |  | V/logic | Digit 1 select |
| A |  | 0(low) |  | V/logic | A segment Out |
| B |  | 0(low) |  | V/logic | B segment Out |
| C |  | 0(low) |  | V/logic | C segment Out |
| D |  | 0(low) |  | V/logic | D segment Out |
| E |  | 0(low) |  | V/logic | E segment Out |
| F |  | 0(low) |  | V/logic | F segment Out |
| G |  | 0(low) |  | V/logic | G segment Out |

Lab3BCD:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Minimum | Typical | Maximum | Units | Description |
| FPGA\_C |  | 0(low) |  | V/logic | On Board Clock |
| S0 |  | 0(low) |  | V/logic | On Board Button, for reset |
| Seg\_1 |  | 0(low) |  | V/logic | Digit 1 select |
| A |  | 0(low) |  | V/logic | A segment Out |
| B |  | 0(low) |  | V/logic | B segment Out |
| C |  | 0(low) |  | V/logic | C segment Out |
| D |  | 0(low) |  | V/logic | D segment Out |
| E |  | 0(low) |  | V/logic | E segment Out |
| F |  | 0(low) |  | V/logic | F segment Out |
| G |  | 0(low) |  | V/logic | G segment Out |

Lab3b:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Minimum | Typical | Maximum | Units | Description |
| FPGA\_C |  | 0(low) |  | V/logic | On Board Clock |
| S0 |  | 0(low) |  | V/logic | On Board Button, for reset |
| Seg\_1 |  | 0(low) |  | V/logic | Digit 1 select |
| Seg\_2 |  | 0(low) |  | V/logic | Digit 2 select |
| Seg\_3 |  | 0(low) |  | V/logic | Digit 3 select |
| Seg\_4 |  | 0(low) |  | V/logic | Digit 4 select |
| A |  | 0(low) |  | V/logic | A segment Out |
| B |  | 0(low) |  | V/logic | B segment Out |
| C |  | 0(low) |  | V/logic | C segment Out |
| D |  | 0(low) |  | V/logic | D segment Out |
| E |  | 0(low) |  | V/logic | E segment Out |
| F |  | 0(low) |  | V/logic | F segment Out |
| G |  | 0(low) |  | V/logic | G segment Out |

Lab3bBCD:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Minimum | Typical | Maximum | Units | Description |
| FPGA\_C |  | 0(low) |  | V/logic | On Board Clock |
| S0 |  | 0(low) |  | V/logic | On Board Button, for reset |
| Seg\_1 |  | 0(low) |  | V/logic | Digit 1 select |
| Seg\_2 |  | 0(low) |  | V/logic | Digit 2 select |
| Seg\_3 |  | 0(low) |  | V/logic | Digit 3 select |
| Seg\_4 |  | 0(low) |  | V/logic | Digit 4 select |
| A |  | 0(low) |  | V/logic | A segment Out |
| B |  | 0(low) |  | V/logic | B segment Out |
| C |  | 0(low) |  | V/logic | C segment Out |
| D |  | 0(low) |  | V/logic | D segment Out |
| E |  | 0(low) |  | V/logic | E segment Out |
| F |  | 0(low) |  | V/logic | F segment Out |
| G |  | 0(low) |  | V/logic | G segment Out |